R&D and Prototyping Plan: SiStrip electronics

RIKEN Strips + LANL Electronics

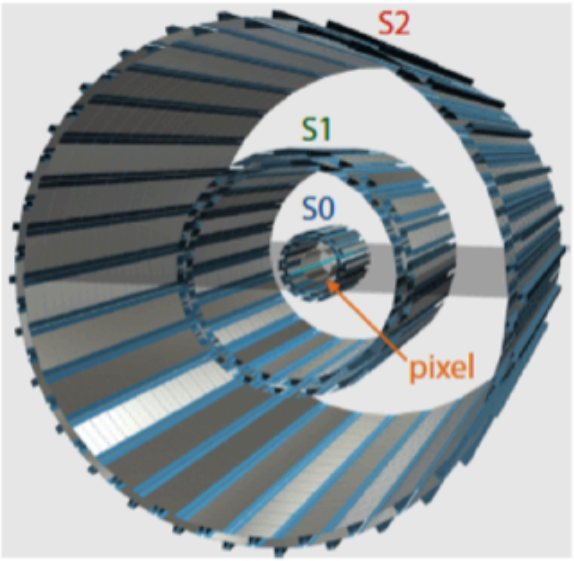
FPHX chip for read-out.

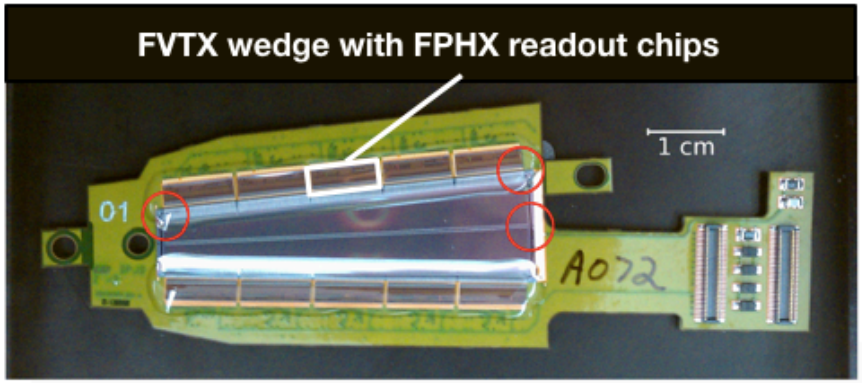
- FPHX is the read-out chip of FVTX
- 128ch/chip. 3bit ADC /ch.
- Low power (64mw per chip)

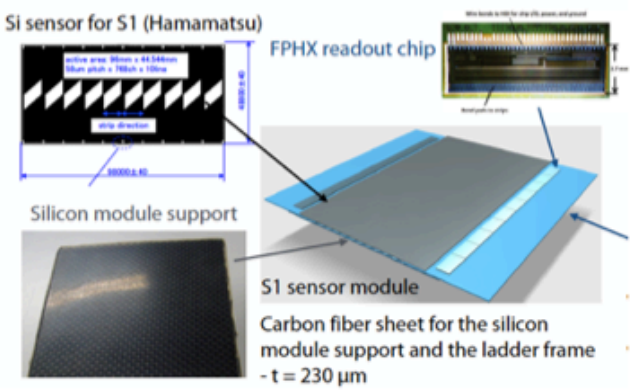
5 strip layers + 2 pixel (more options later)

S2: 1 strip layer at R~60 cm ~1% X0 (2% in ref. design)
S1ab: 2 strip layer at R~34 cm ~1% X0 total (2% in ref. design)
S0ab: 2 strip layer at R~ 8 cm ~1% X0 total (2.7% in ref. design)
P1: pixel at R~5 cm (reconfigured VTXP) 1.3% X0
P0: pixel at R~2.5cm (reconfigured VTXP) 1.3% X0

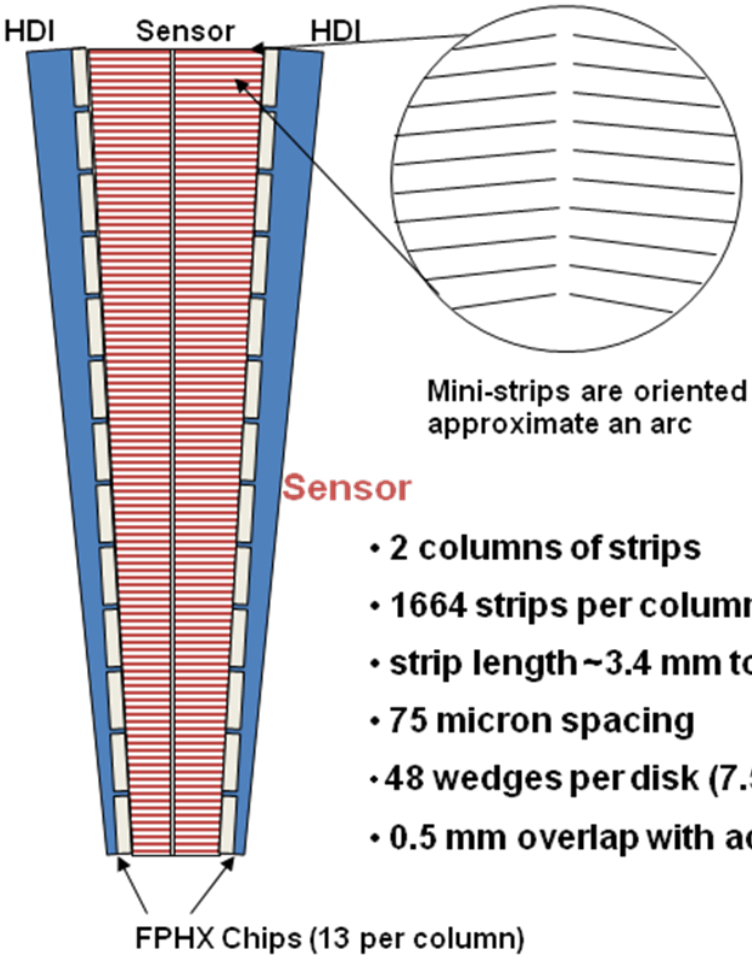
- All strips are 75 μm x 9.6mm. S0b has a small stereo angle.
- Overall material is ~5.6% radiation length.
- Air cooling to achieve small radiation length
- Small rad. length enables smaller over-all size and to keep the required momentum resolution to separate 3 Upsilon states
- S0+S1+S2: ~8m^2 of silicon and 3.2M ch





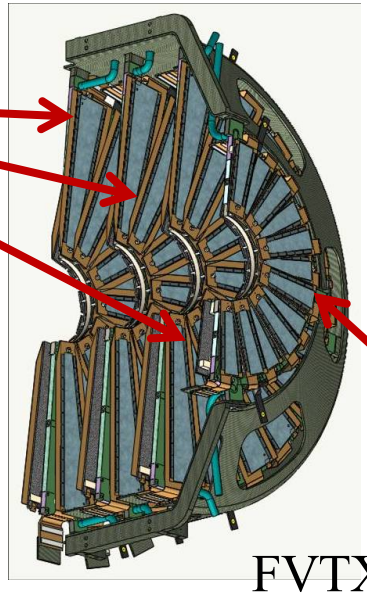


FVTX Sensor Long Wedge



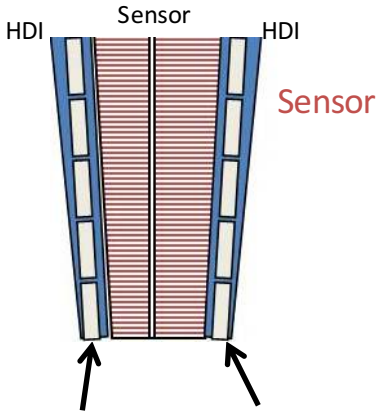
- 2 columns of strips
- 1664 strips per column
- strip length ~3.4 mm to ~11.5 mm
- 75 micron spacing
- 48 wedges per disk (7.5°/sensor, 15°/wedge)
- 0.5 mm overlap with adjacent wedges

Overall length 126.8 mm
Overall width 8.8 mm i.r., 25.4 mm o.r.



4 hermetic disks, z =18.5 to 38 cm

FVTX Sensor Short Wedge



Overall length 50.1 mm
Overall width 8.8 mm i.r., 15.3 o.r

Readout Chip Layout

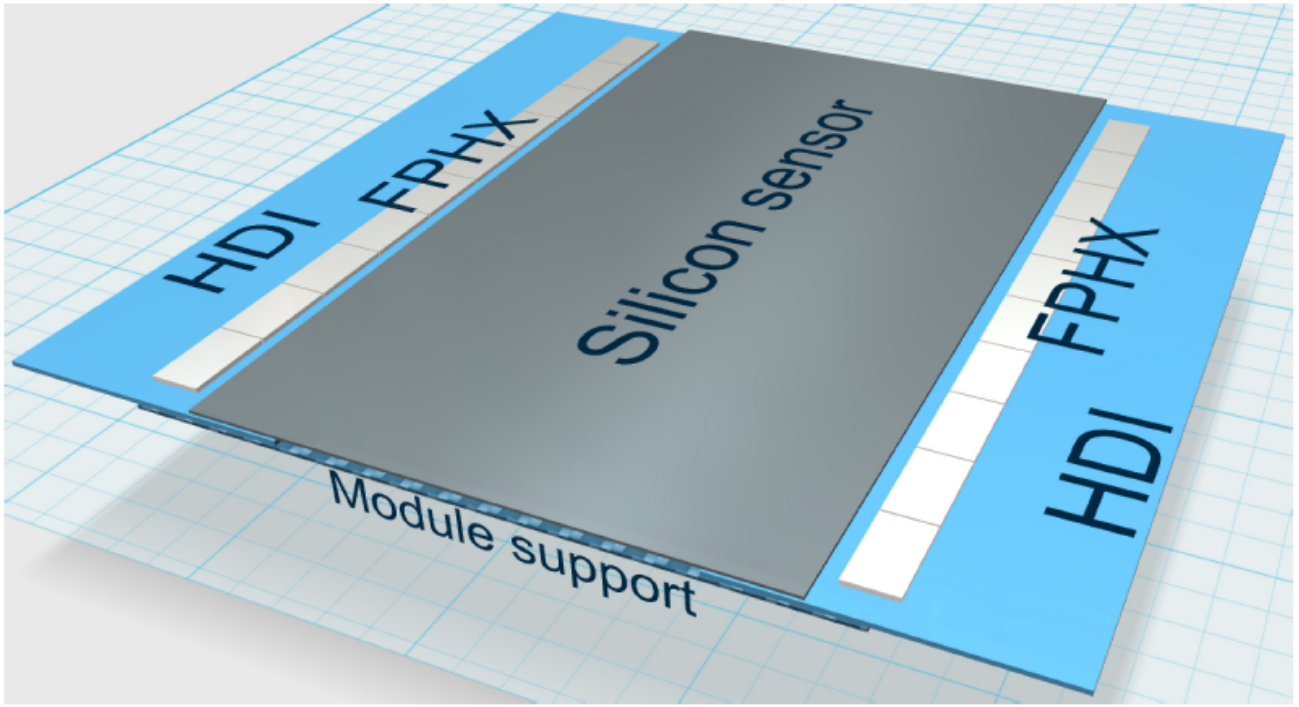
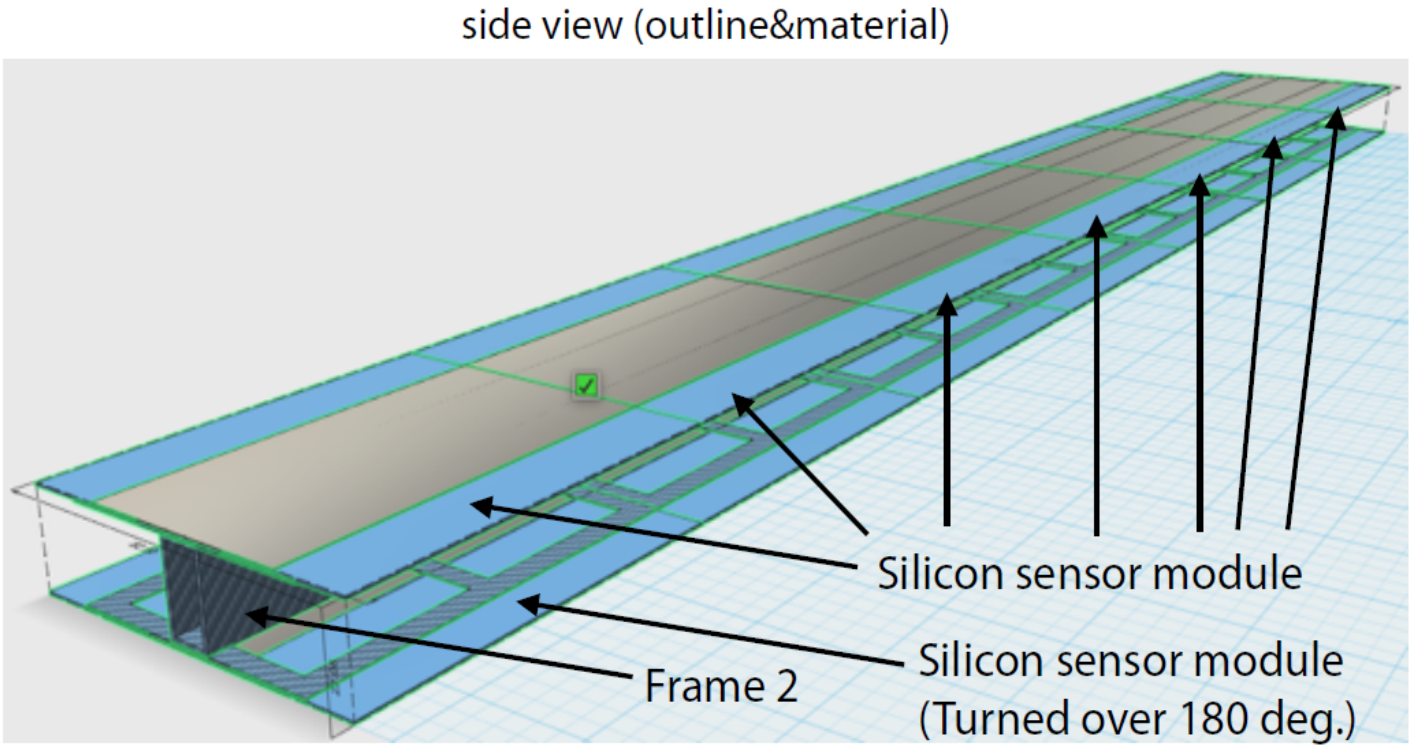


Figure 4.48: Layout for the silicon sensor module for the S1 detector.

Dual Sided Ladder Arrangement



Silicon strip tracker in pCDR

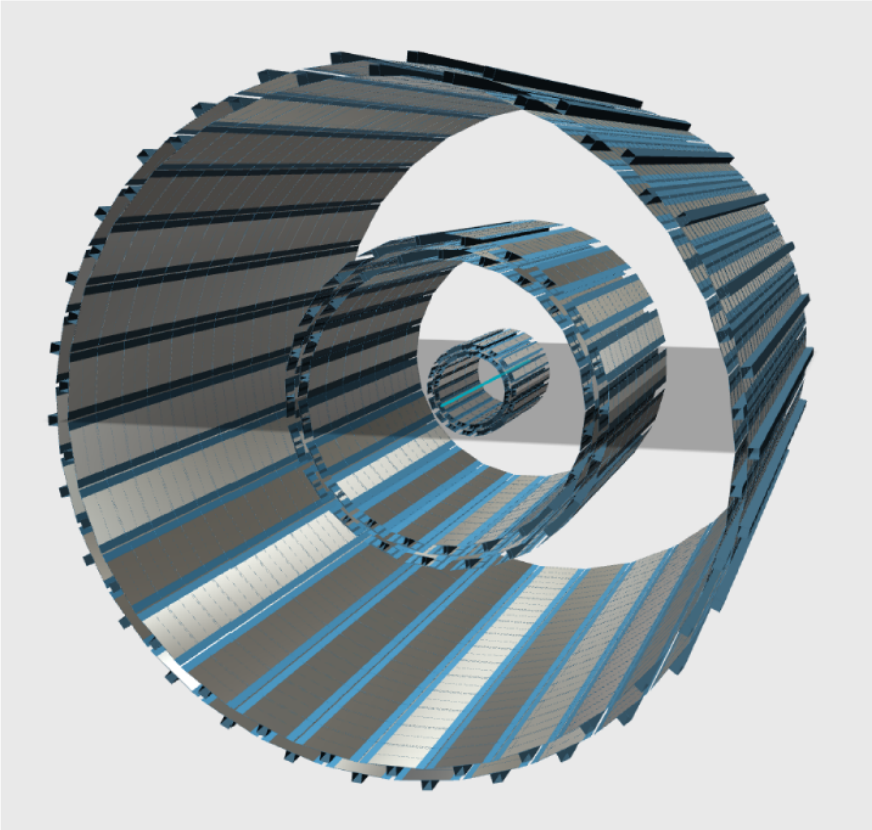
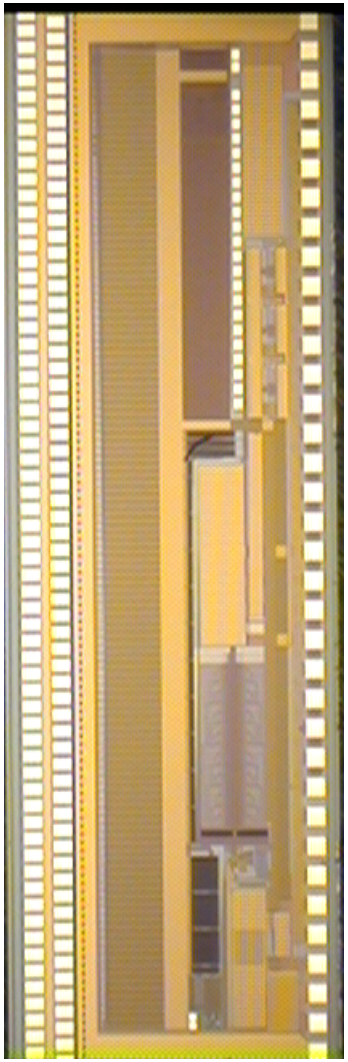


Figure 4.1: CAD drawing of the silicon strip tracker.

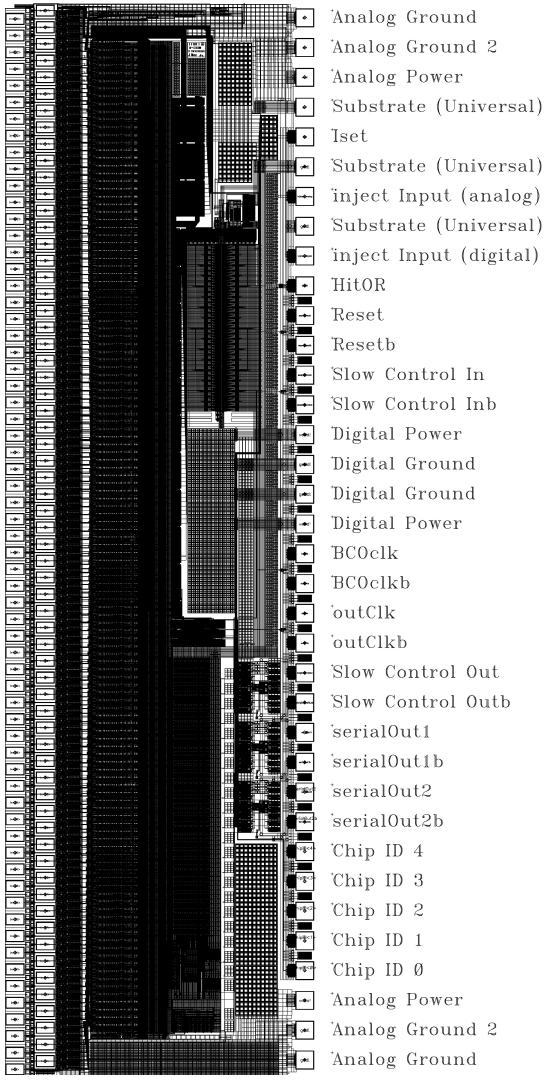
The FPHX Chip

The FPHX is the custom readout chip designed for the FVTX Silicon Sensor. Each FPHX chip integrates and shapes (CR-RC) signals from 128 channels of mini-strips, digitizes and sparsifies the hit channels each beam crossing (106ns beam clock), and serially pushes out the digitized data.

Photo



Layout

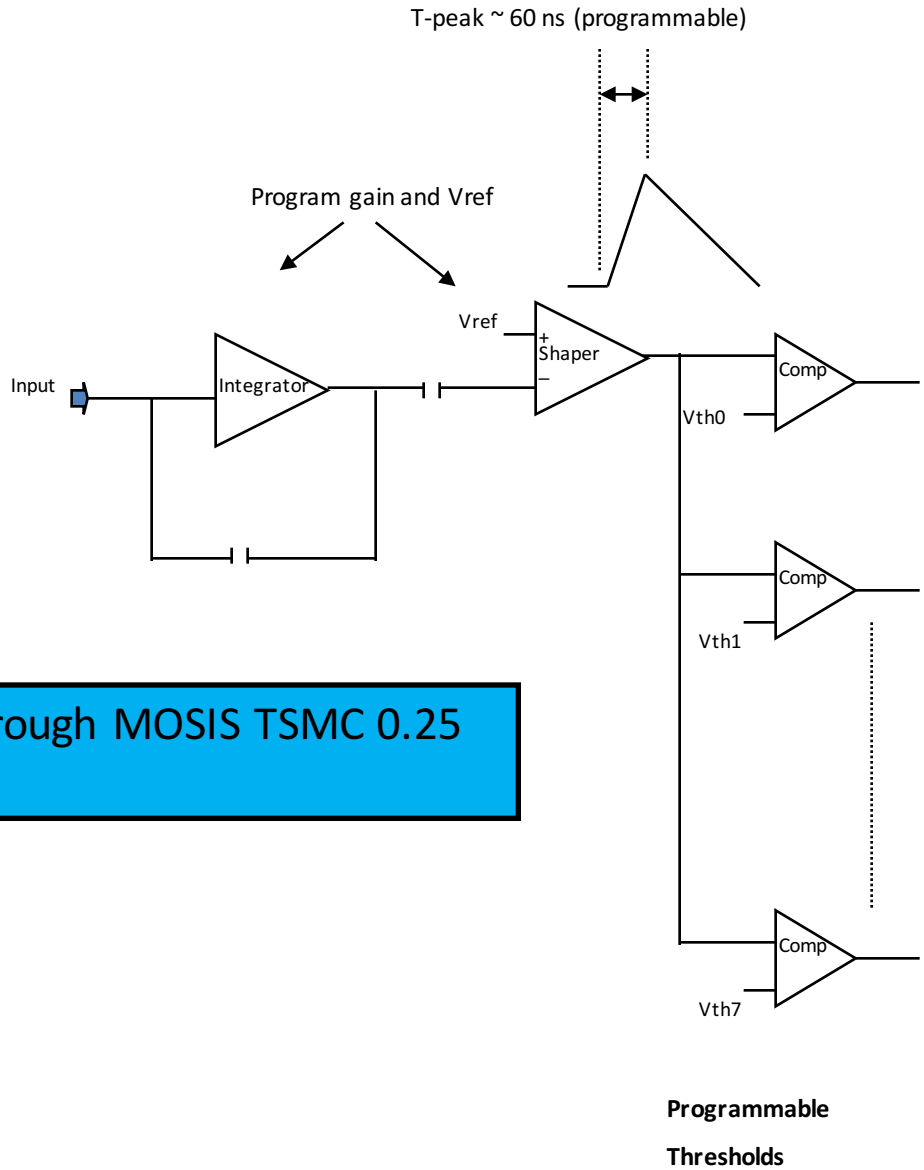


The FPHX is a mixed-mode chip with two major and distinct sections, the front-end and the back-end.

FPHX readout chip front end

- 128 channel
- 46 to 200 mV/fC
- 60 ns peak time (programmable)
- 3—bit ADC (programmable)
- Optimized for 1 to 2.5 pf
- 115e + 134e/pf
- ~ 70 to 140 uW/ch (dep. Bias current)

Fully functional chip design submitted through MOSIS TSMC 0.25 micron process



Front-end Specifications

Configuration: 128 identical channels. Each channel contains a charge integrator, shaper, programmable threshold discriminator, and an 8-comparator thermometer ADC with fully programmable thresholds.

Input charge signal polarity: positive (holes)

Input capacitance: the design is optimized for an external detector capacitance of approx. 1.5pF (and estimated chip parasitic C of 0.5pF)

Detector leakage current compensation: programmable maximum of 0 – 100nA

Effective Channel gain: 46, 50, 60, 67, 85,100, 150, or 200 mV/fC (programmable)

Output: 3-bit digital code per channel (digitized shaper output pulse height). No analog output.

Output pulse dynamic range (shaper output): >800mV (25ke to 100ke, depending on the gain setting)

Nominal output pulse peaking time: 60 ns (programmable, set by the shaper)

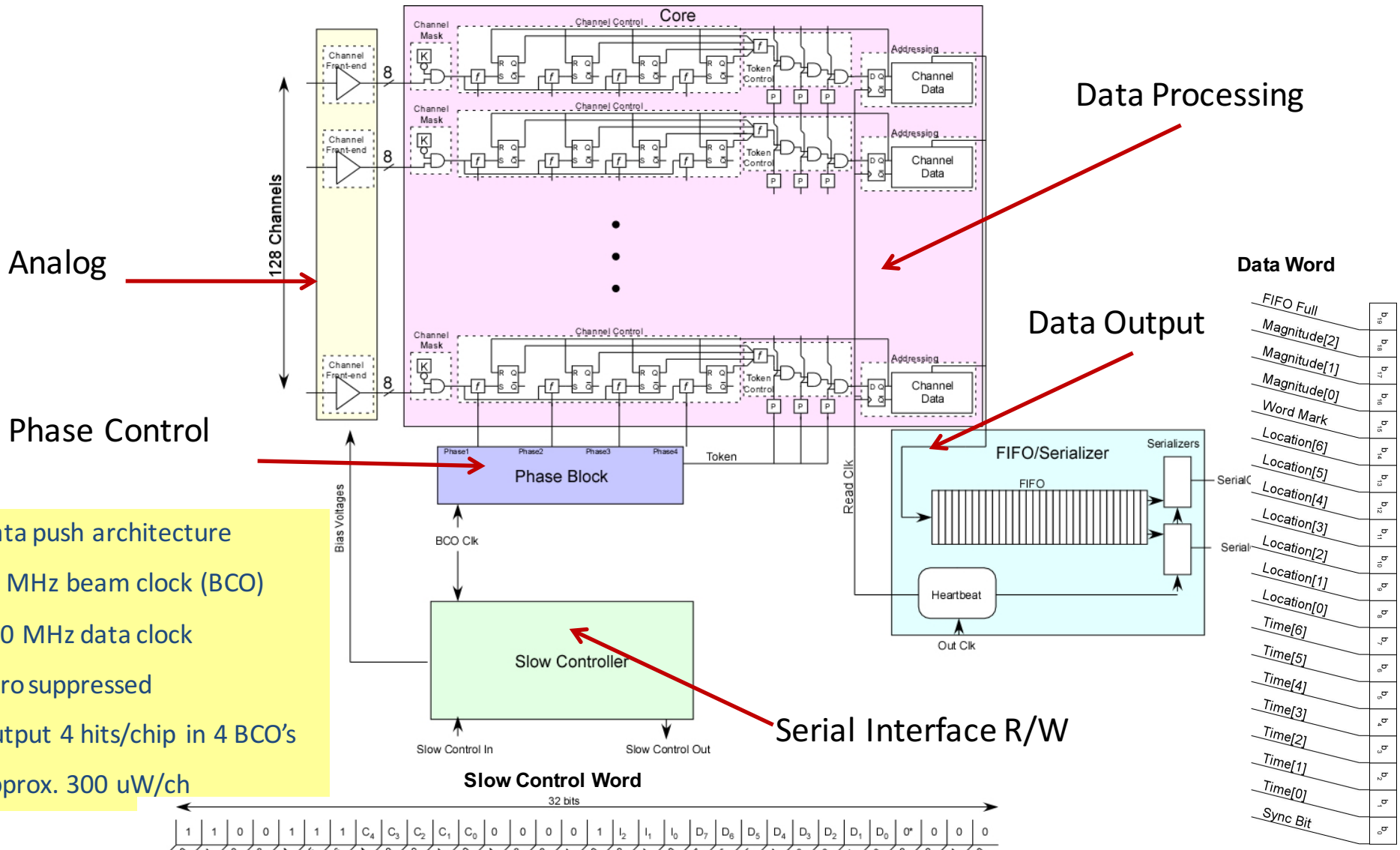
Output pulse fall time: programmable, set by the integrator fall time adjust

Noise at shaper output: 115e + 134e/pf (simulation)

Power: Approx. 140 uW per channel for the maximum input transistor bias current of 38uA, approx. 300 uW per channel for the back end.

2 test pulse inputs: one direct analog, one controlled by a DAC and digital input.

FPHX Chip back-end organization



- Data push architecture
- 10 MHz beam clock (BCO)
- 200 MHz data clock
- Zero suppressed
- Output 4 hits/chip in 4 BCO's
- Approx. 300 uW/ch

Back-end Features

- Up to 4 hit strips can be read out in 4 beam clock cycles (4 x 106 ns)
- Hits are processed in a 4-phase architecture
- Access to the readout bus is controlled by token logic
- Data is pushed onto one or two LVDS serial outputs lines (user selected)
- Data output word is 20 bits
- Output word includes channel ID, 3-bits ADC, time stamp
- Sync word is provided to synchronize DAQ, 1 “sync bit” followed by 19 zeroes
- Serial data output clock is 200 MHz
- Channels can be masked off in any pattern (programmable)
- Output data is zero-suppressed
- FIFO is 20 bits wide and 32 words deep
- Slow control is a serial read/write interface to the FPHX, 32-bit word, clocked at 10 MHz

FPHX Chips –

- **Required: (26x48x6) + (10x48x2) = 8,448 chips installed**
- **Assume 10% spares: 845 chips**
- **Required with spares: ~9300 chips**
- **Chip/wafer estimate from Ray (2007): 1088 chips/wafer (approximately 85% reticle-to-wafer area)**
- **Initial minimum production wafer guarantee: 10 wafers, 10,880 chips**

Assume 80% yield: 8704 usable chips, 3% spares
Assume 85% yield, 9248 usable chips, 9.5% spares
Assume 90% yield: 9792 usable chips, 16% spares

A reply has been posted for the following MOSIS Customer Support inquiry.

Subject: Masks for project number 81650
Category: Other Issues
From: zimmerman@fnal.gov
Updated: 15-Oct-2015 10:33
Inquiry: 23895

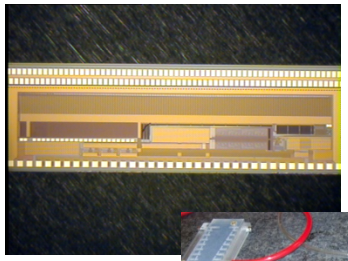
Our response to your inquiry is below. You may also view this in context by connecting to the URL above and entering the password to your MOSIS customer support account.

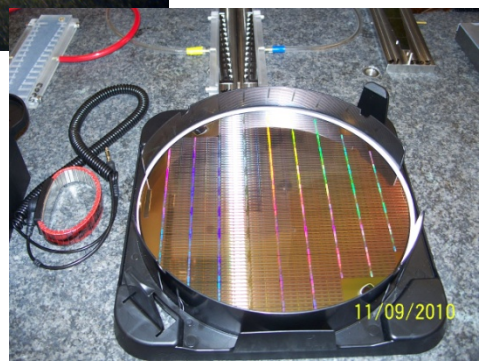
Project 81650 (Run T9BD) was fabricated under account number 598.
That is why you do not see a record of this project on your account (#573) page.

The masks are still available.

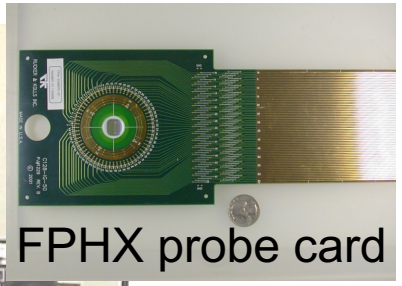
Best Regards,
MOSIS Support

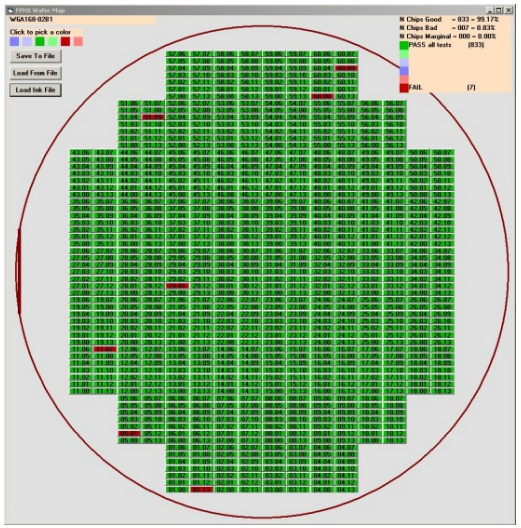
The FPHX Chip





All major functions of the FPHX tested on the wafer probe station. One wafer per day. Greater than 95% yield.





- FNAL designed FPHX-specific probe card
- FNAL developed control software to run the probe station
- FNAL developed software to run test program on the probe station
- All registers written to and read back
- Pulser scan tests run for each die
- Bad chips were inked
- All test results written to a database

Backup Slides

CORWIL Dicing Instructions for FPHX Wafers

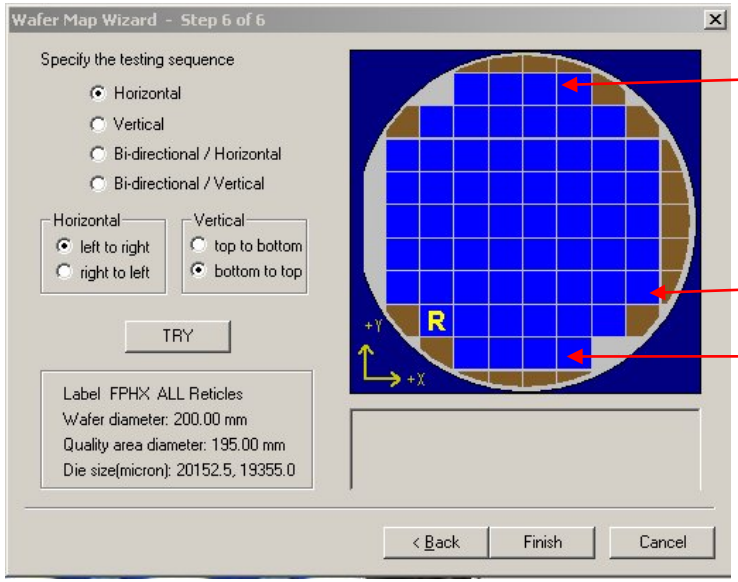


Figure 1. FPHX Reticules on the 8" wafer.

1. **There are 60 full reticules on wafer – see the blue squares in Figure 1. All die within these reticules will be pack in waffle packs.**

2.There are 19 partial reticules on wafer – see the brown squares in Figure 1. All die within these reticules will be left on blue tape and shipped back.

3.The reticules are tested and numbered as shown in Figure 1: First direction is horizontal, from left to right; second direction is vertical, from bottom to top.

4.The 60 full reticules contain 14 sites, each with one die – see Figure 2. The die inside a reticule is tested and numbered from 0 to 13. The left column contains, from bottom to top, die number 0 to 6. The right column contains, from top to bottom, die number 7 to 13.

5.The 840 die will be placed in waffle packs based on their reticule number (1 to 60) and site number (0 to 13). We need to be able to keep track of each die identification numbers.

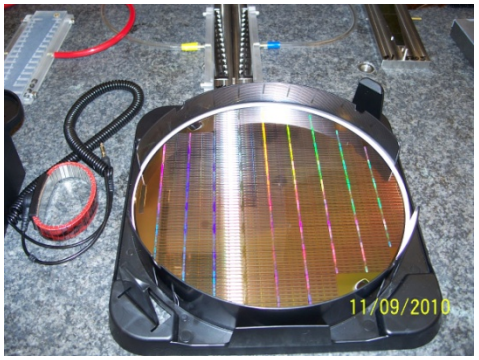
6.Each wafer is accompanied by a map as shown in Figure 3. Each die has a reticule number and site number as described. Both good die (green color) and bad die (red color) must be harvested in waffle packs.

FPHX Schedule

24 production wafers (approx. 20,000 die)

8448 installed in FVTX

~13,000 tested die available for assembly



WBS	item	Date
1.4.2.3	FPHX layout design	04/10/08 done
1.4.2.6	Design review	04/14/08 done
1.4.2.4.1	Submission to MOSIS	06/22/08 done
1.4.2.4.2	Prototype tests	10/10/08 done
1.4.2.4.3, 1.4.2.4.4	Submit second prototype run	06/16/09 done
1.4.2.4.5	Test second prototype	09/25/09 done
1.4.2.4.9	Second run performance review	10/01/09 done
1.4.2.5.1	Submit engineering run (production run)	12/17/09 done
	Receive production Wafers	01/06/2010 done
1.4.2.5.2	Test production wafers	05/14/10 done
	Dice Production wafers	07/09/10 done

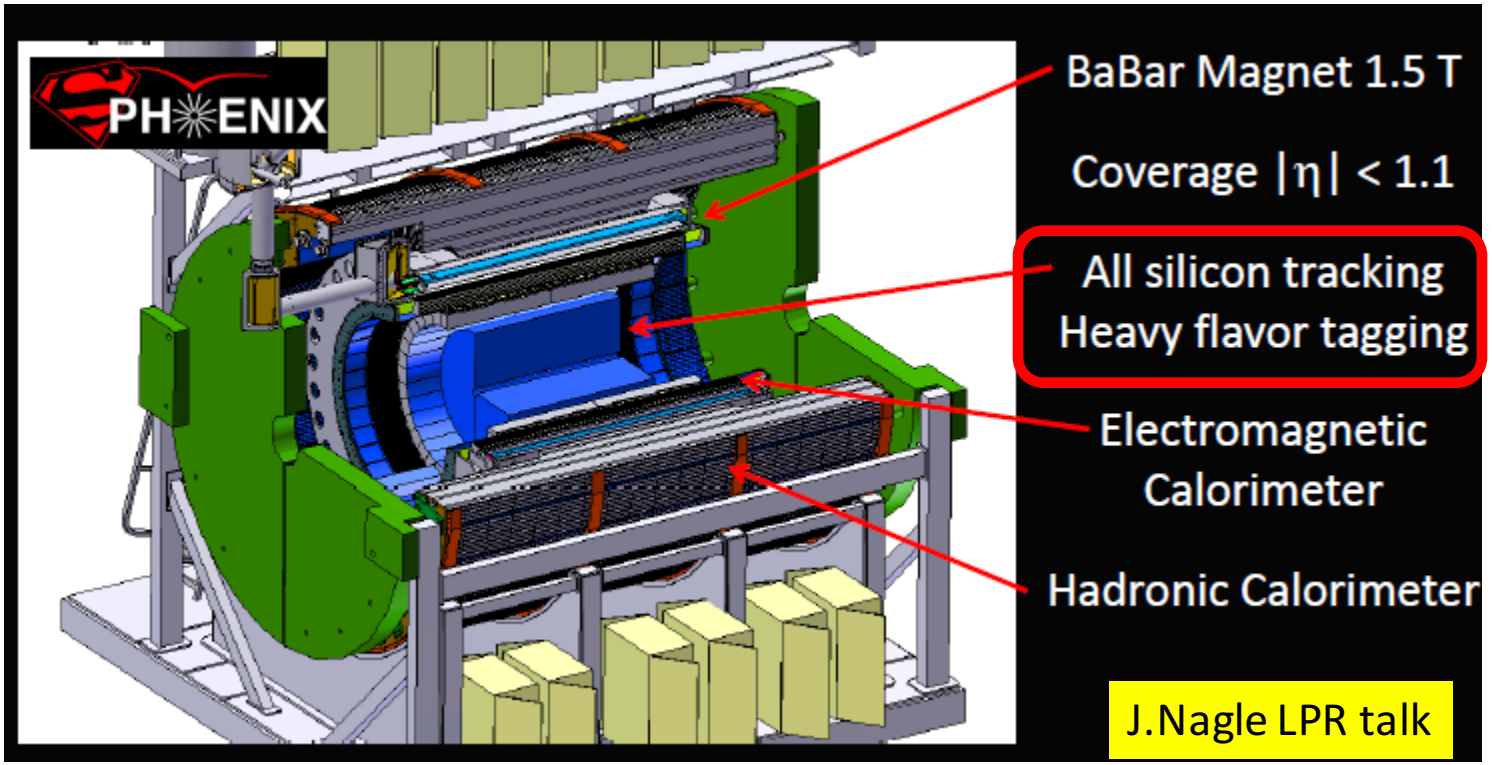
Design Decisions Leading to the FVTX Sensor Wedge and FPHX

Technical risk minimization the key driver

- **Mini-strips maintain good resolution in r and phi with reasonable occupancy and manageable channel count**
- **Wire bonds replace initial idea to use bump bonds**
- **Chip placement moved from centerline of sensor to the edges**
  - **minimizes potential noise coupling between chip and sensor**
  - **facilitates implementation of decoupling between sensor bias and chip reference and avoids long path-length sensor return to ground**

- **Wedge assembly unit based on ease of assembly**
- **Readout architecture of the FPHX draws on previous successful designs; FPIX2, FSSR, and the SVX family of readout chips (0.25 micron TSMC CMOS process)**
- **Low power design of the FPHX simplifies cooling and mechanics significantly**

Reference design and requirements



- $|\eta|<1$ and $\Delta\phi=2\pi$
- High efficiency & purity in central Au+Au to measure modified FF
- High rate (15kHz DAQ)
- High momentum resolution to separate Upsilon states
- Precision vertex measurement for heavy flavor measurements (D, B→J/Psi, b-tagged jets)
- Compact (Fit inside of EMCAL)

Basic design philosophy

- Use technology we are familiar with
  - Minimize the development cost
  - Minimize the cost and schedule risk
  - Little “R”, only “D”
  - Complete the system on time (2020)
- Minimal system that satisfies the physics requirement to minimize the cost in terms of money and the manpower, and to minimize the schedule risk
- Current model
  - AC coupled, single-sided, strip sensor
  - No stereo angle
  - Outer radius ~ 60cm (for 100MeV resolution of Upsilon)
  - FPHX readout

Silicon tracker model in pCDR

- FPHX chip for read-out.
  - FPHX is the read-out chip of FVTX
  - 128ch/chip. 3bit ADC /ch.
  - Low power (64mw per chip)
- 5 strip layers + 2 pixel

  S2: 1 strip layer at R~64 cm ~1% X0 (2% in ref. design)

  S1ab: 2 strip layer at R~32 cm 1.2% X0 total (2% in ref. design)

  S0ab: 2 strip layer at R~ 8 cm ~2% X0 total (2.7% in ref. design)

  P1: pixel at R~5 cm (reconfigured VTXP) 1.3% X0

  P0: pixel at R~2.5cm (reconfigured VTXP) 1.3% X0
  - All strips are 60 or 58 μm x 9.6mm. No stereo
  - Overall material is ~4.2% (+ 2.6% pixel) radiation length.
    Most of them (~3%+2.6%) are near beam or in the last layer
  - Air cooling to achieve small radiation length
  - Small rad. length to make small over-all size and to keep the required momentum resolution to separate 3 Upsilon states
  - S0+S1+S2: ~10m^2 of silicon and 3.1 M ch

Current design in pCDR

Station	Layer	radius (cm)	pitch (μm)	sensor length (cm)	depth (μm)	total thickness X_0%	area (m^2)
Pixel	1	2.4	50	0.425	200	1.3	0.034
Pixel	2	4.4	50	0.425	200	1.3	0.059
S0a	3	7.5	58	9.6	240	1.0	0.18
S0b	4	8.5	58	9.6	240	1.0	0.18
S1a	5	31.0	58	9.6	240	0.6	1.4
S1b	6	34.0	58	9.6	240	0.6	1.4
S2	7	64.0	60	9.6	320	1.0	6.5

Table 4.2: Number of channel summary for the silicon strip tracker.

station	sub-layer	silicon modules per ladder	# of ladders	# of sensors
S0	2	3	36	216
S1	2	7	44	616
S2	1	14	48	672

Simulation of the current design (in pCDR)

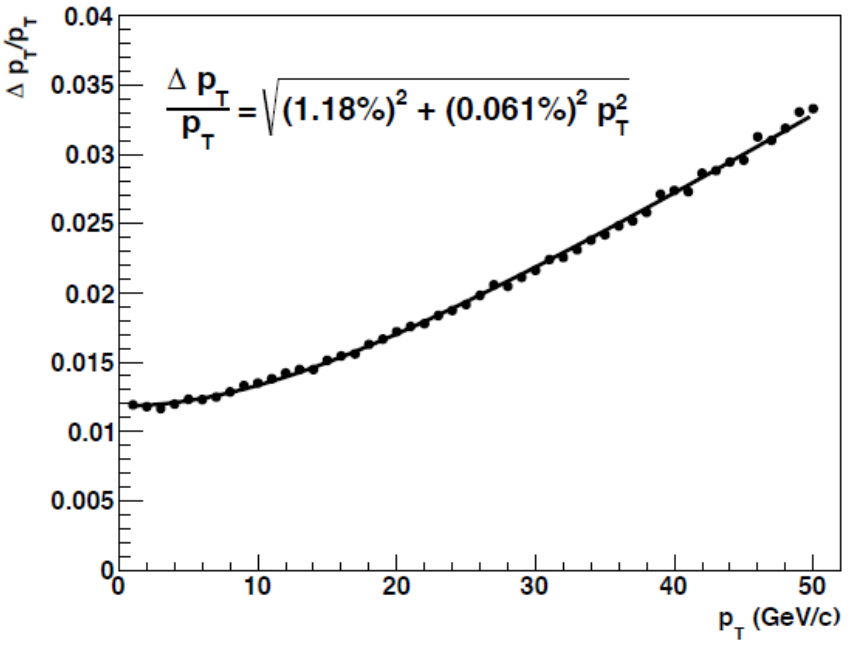


Figure 4.41: Momentum resolution of the silicon tracker for single pic

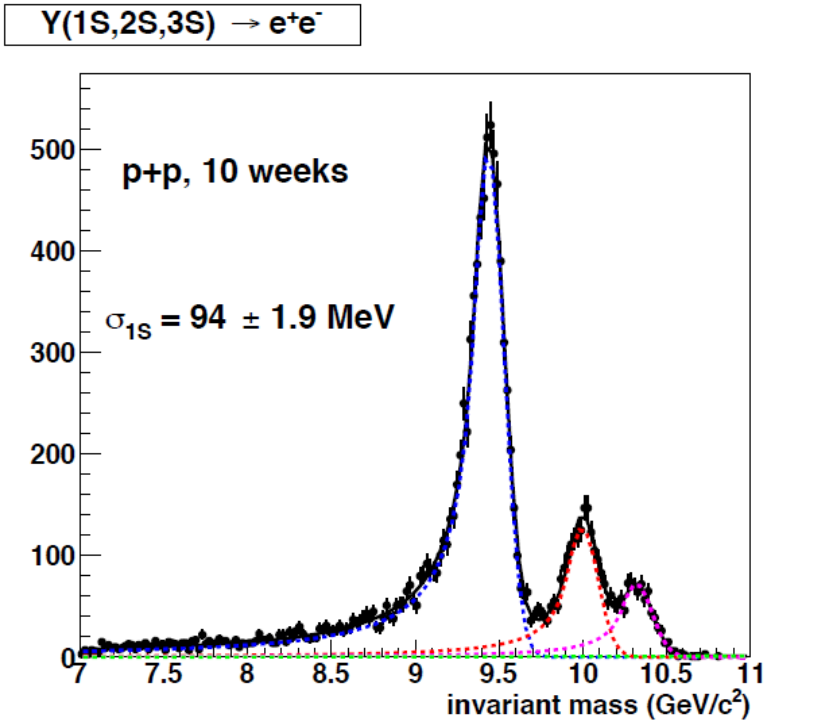


Figure 4.42: Mass spectrum of the three Upsilon states, with Crystal Ball fits.

- Expected momentum resolution and mass resolutions for Upsilon calculated by Tony Frawley for preliminary Conceptual Design Report
- σ=94 MeV for Upsilon. Three upsilon states are clearly separated

Concept of Sensor (for S2)

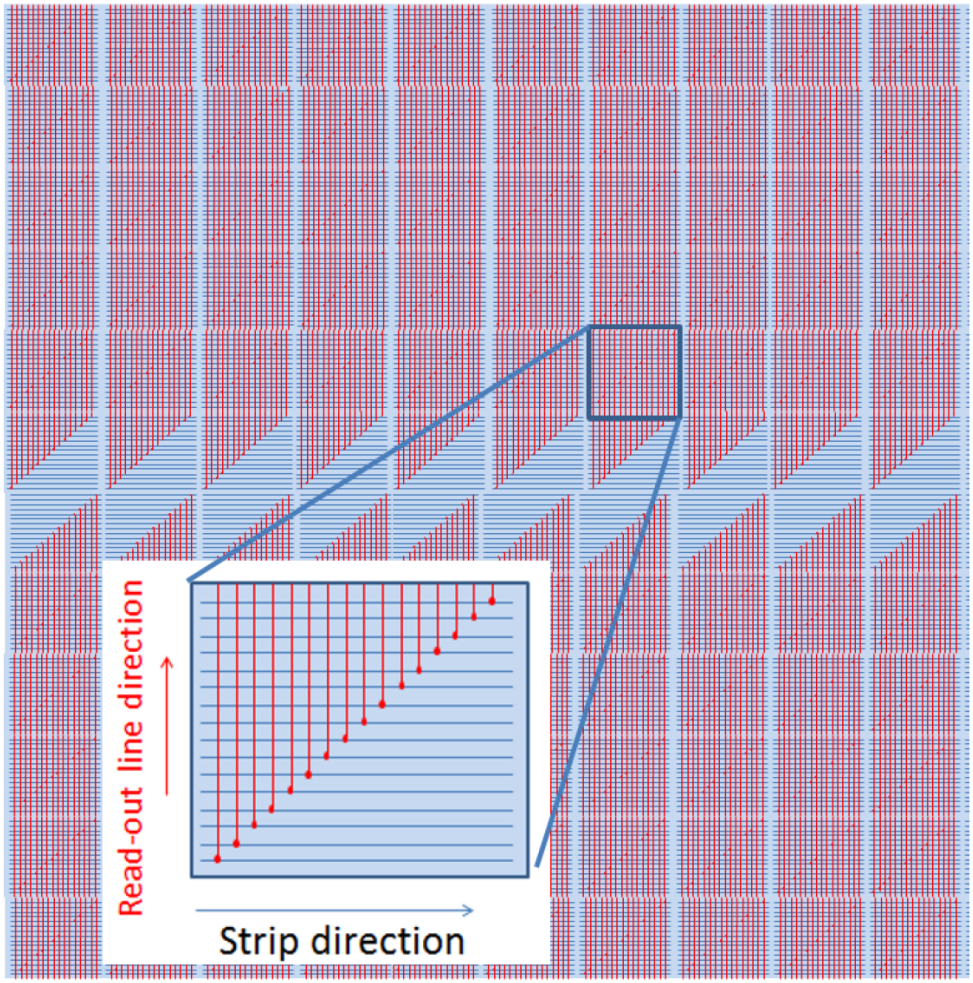


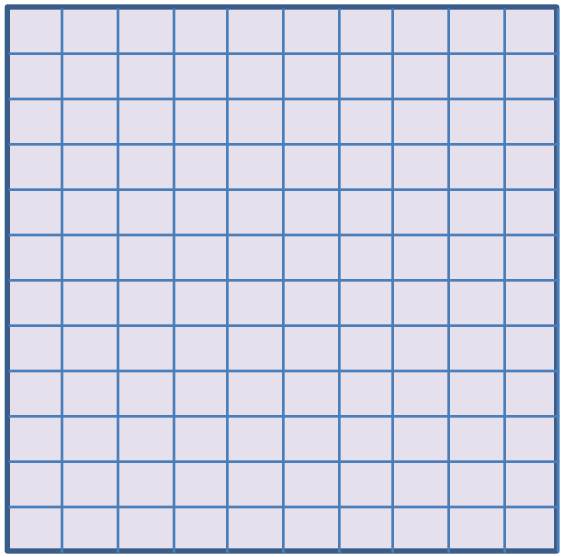
Figure 4.3: Schematic layout strip and readout lines of the sensor.

- 96mmx92.16mm active area
- Divided into 10x12 blocks
- Each block is 9.60mm x 7.68mm and made of 128 strips of 9.6mm x 60 micron
- Upper 6 bocks are connected upwards.
- Lower 6 blocks are connected by downwards
- 24 FPHX chips to read-out the entire sensor

3 sensors for strip layers

S2 sensor

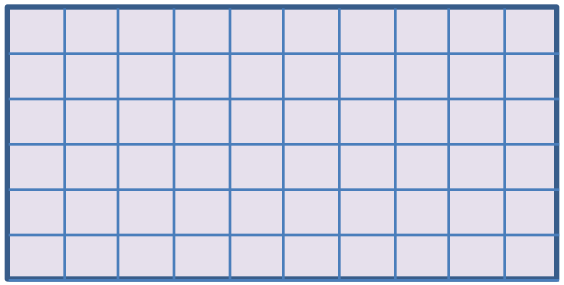
Bonding pads for 10 FPHXs



Bonding pads for 10 FPHXs

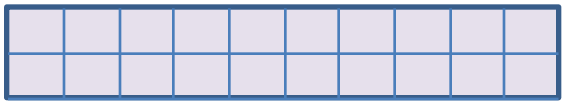
S1 sensor

Bonding pads for 10 FPHXs



Bonding pads for 10 FPHXs

Bonding pads for 10 FPHXs

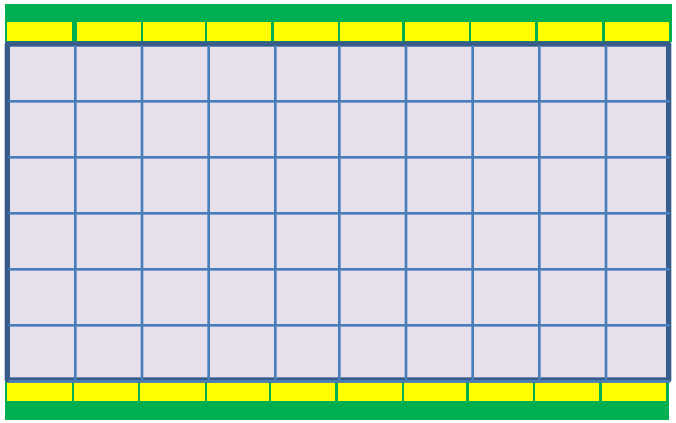


Bonding pads for 10 FPHXs

- Each sensor is divided in cells of 9.6m(z)x7.68mm active area. Each cell consists of 128 strips of 60μm x 9.6mm
- S2, S1, S0 sensors are made of 12x10, 6x10, and 2x10 cells, respectively
- 1 ch in S2 read 6 strips and 1 ch in S1 read 3 strips to save channel counts. Channel occupancy is ~0.2% in S1 and 0.1% in S1 in central Au+Au.

Concept of FPHX based module (S1)

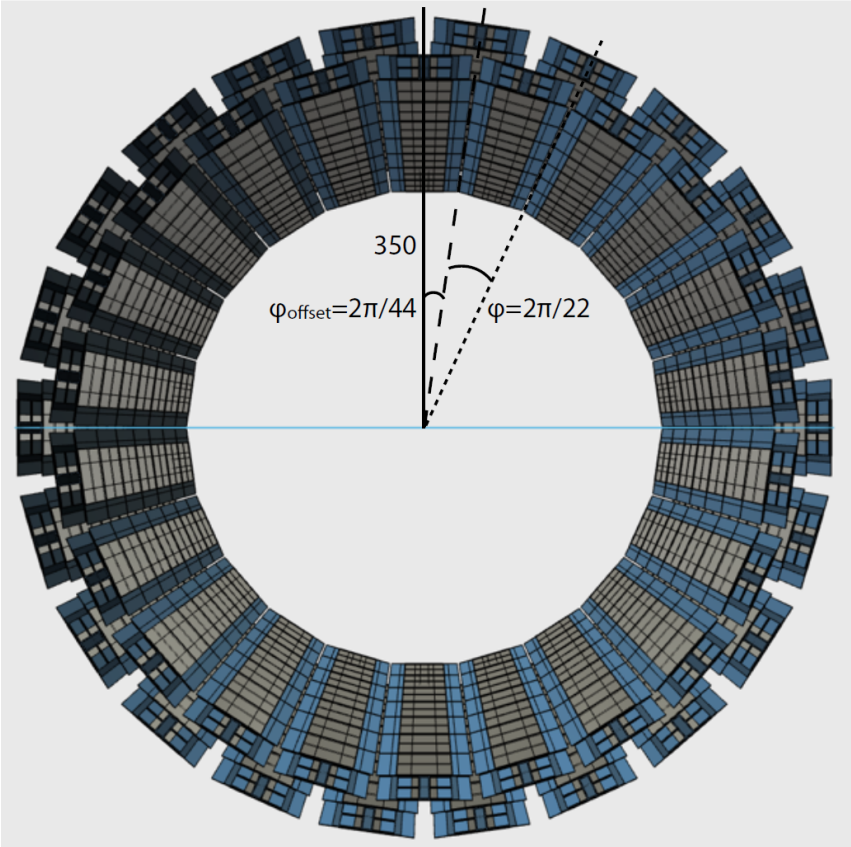
HDI of 10 FPHX chip

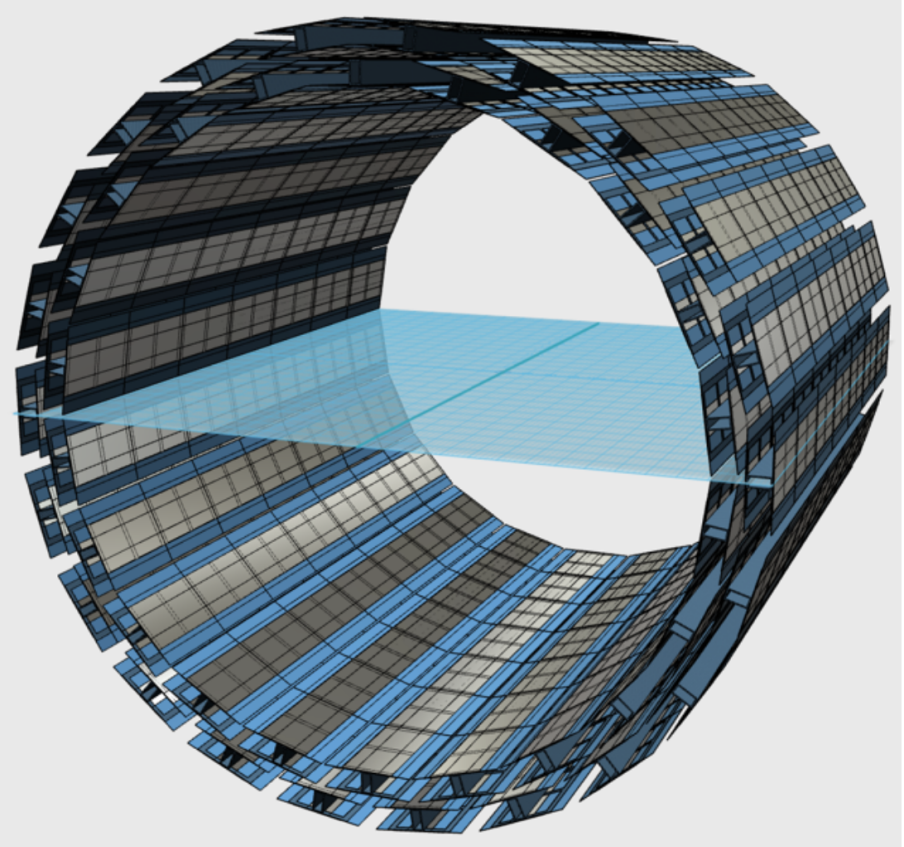


HDI of 10 FPHX chip

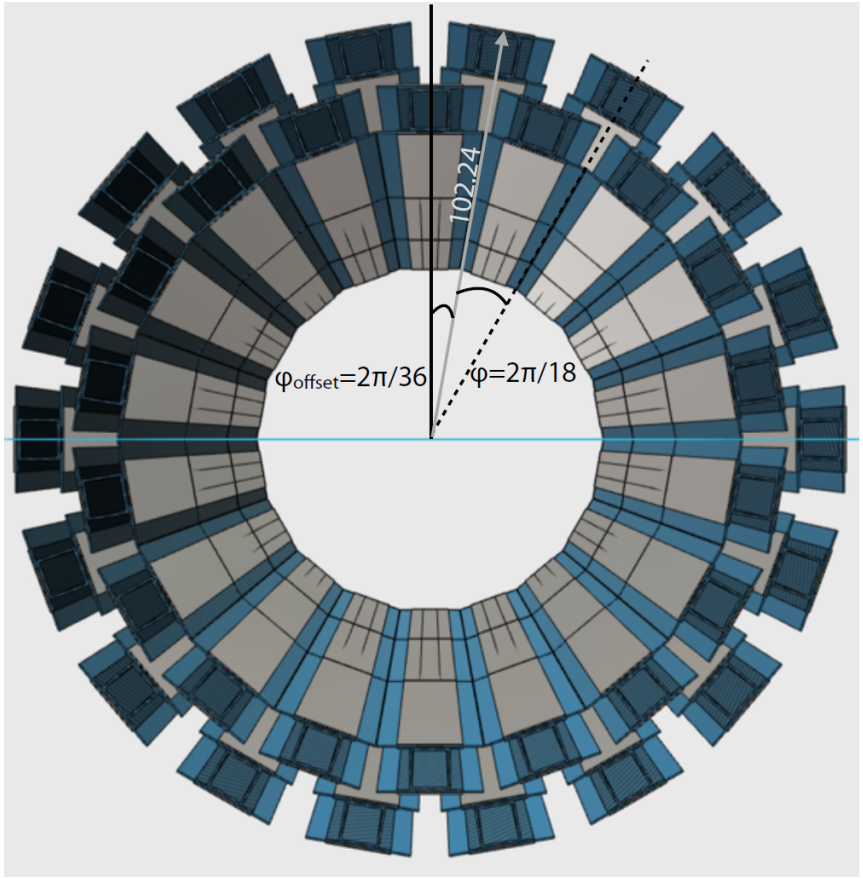
- This is a concept of a sensor module with FPHX read-out
- It is made of
  - Sensor of (6 x 10) cell structure. Each cell has 128ch of 58 um x 9.6mm strips
  - A “ROC” (or “HDI”) of 10 FPHX chips. They are attached at the top and the bottom of the sensor
  - The “HDI” is electrically equivalent to the “small HDI” of FVTX so that it can be read-out by a FVTX test bench

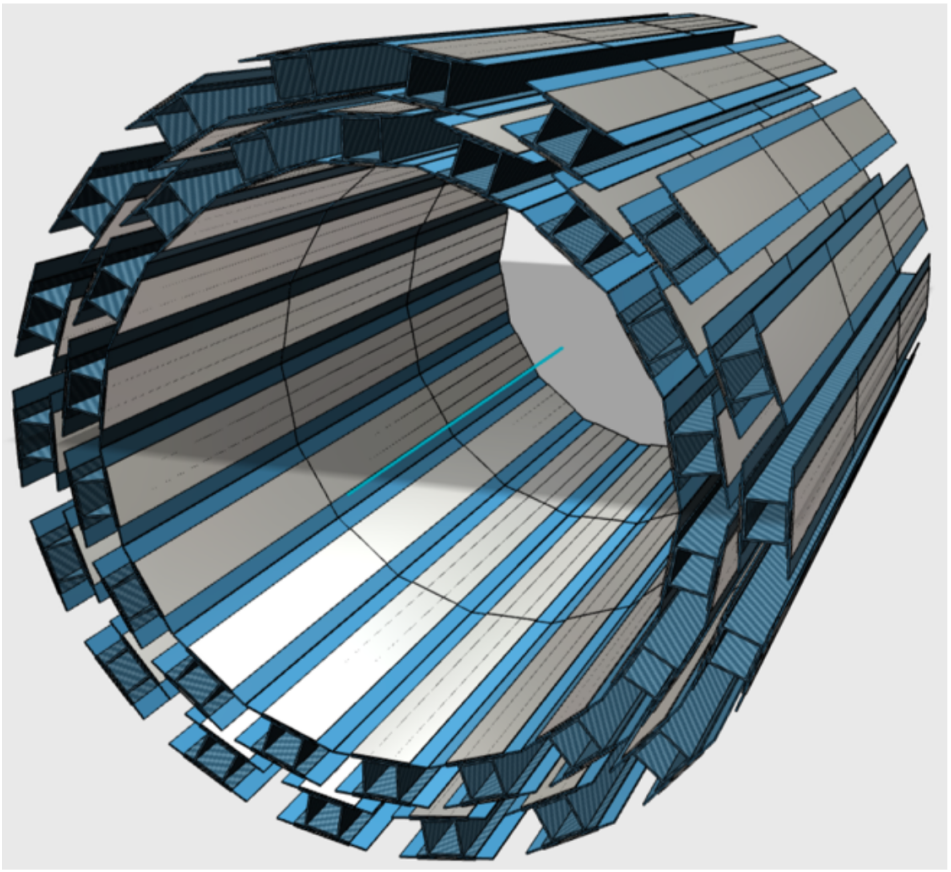
S1 barrel (R=30-35cm)



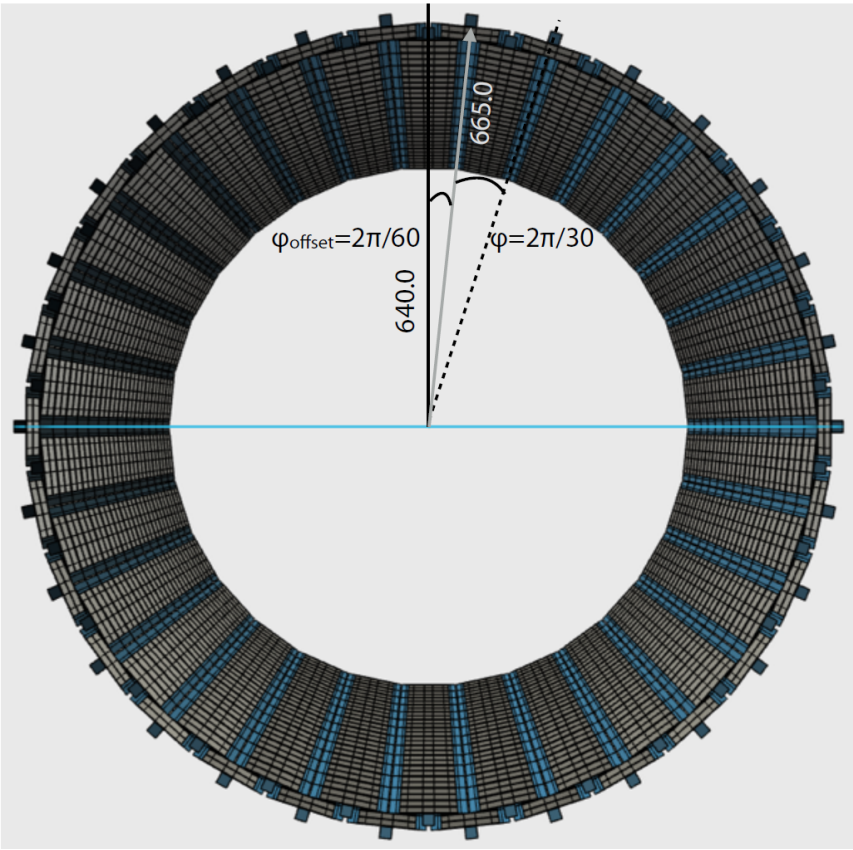


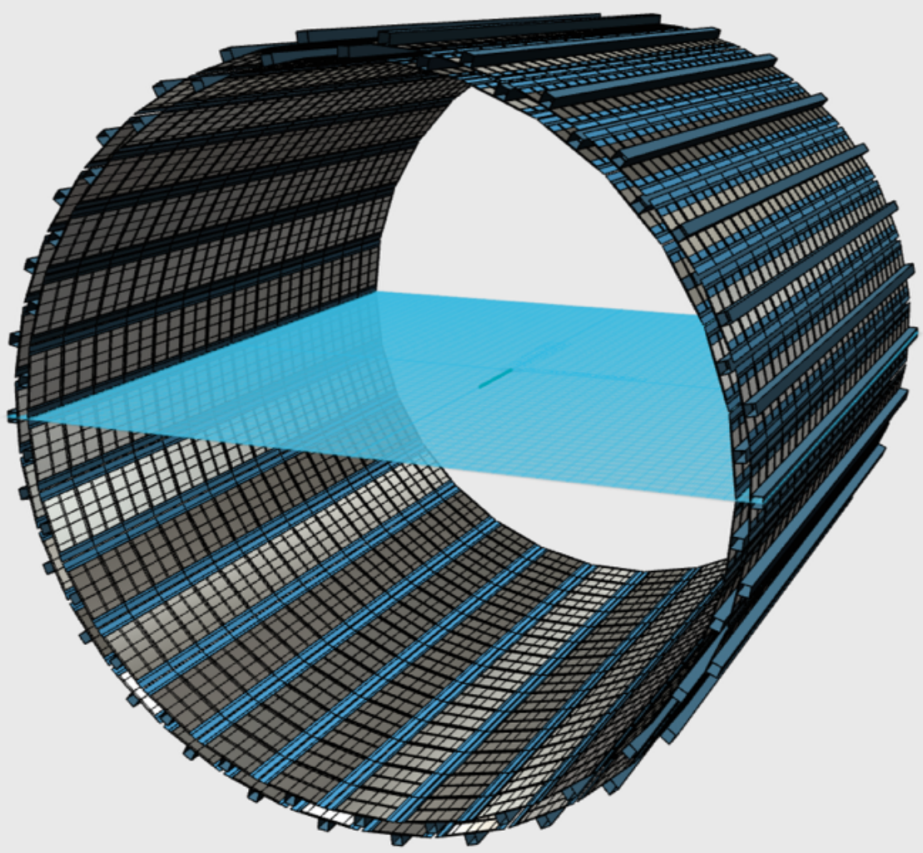
S0 barrel (R~8cm)



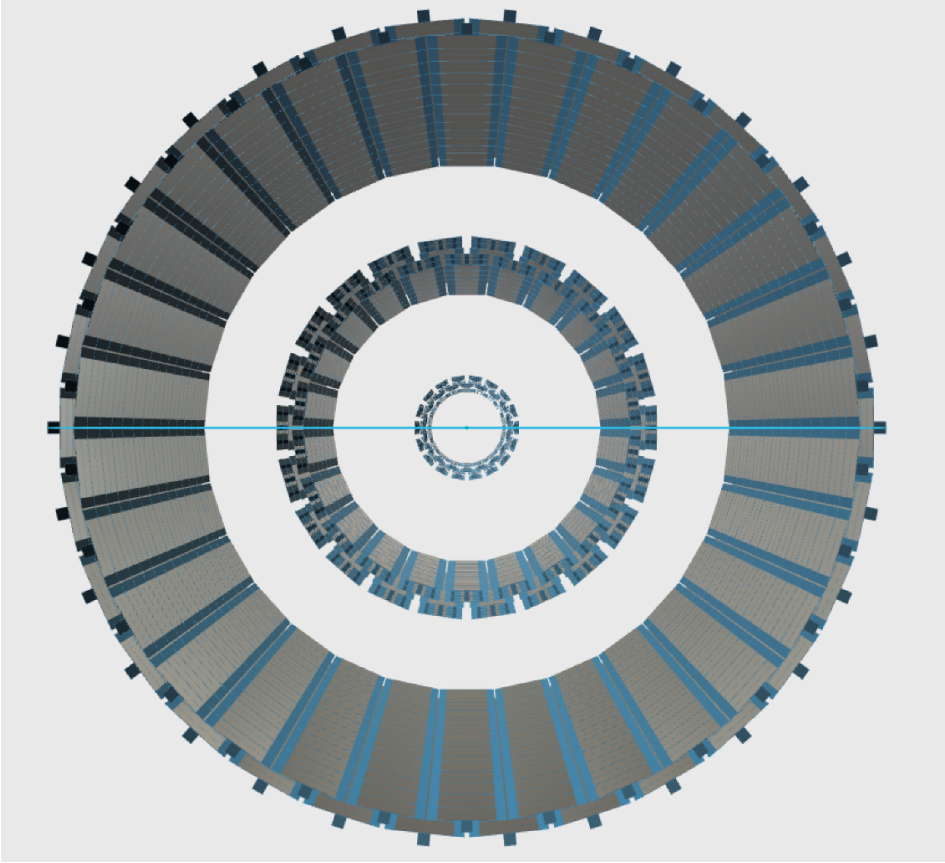


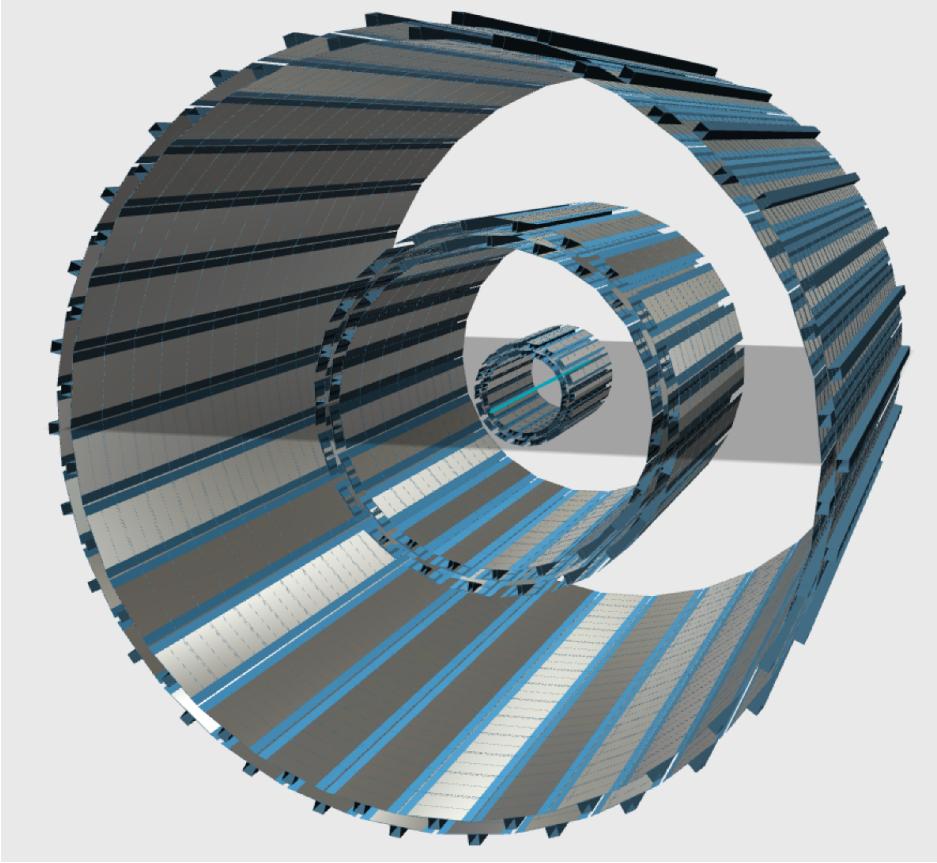
S2 (R~65 cm)





S0, S1, S2 barrels





Time line of the project

ID	WBS	Task Mode	Task Name	Start	Finish
1	**1.4**		**Tracker**	**Mon 8/24/1**	**Fri 5/17/19**
2	**1.4.1**		**Tracking Management**	**Mon 8/24/1**	**Fri 5/17/19**
3	1.4.1.1		start	Mon 8/24/1	Mon 8/24/1
4	1.4.1.2		end	Fri 5/17/19	Fri 5/17/19
5	**1.4.2**		**VTX reconfig**	**Mon 8/24/1**	**Fri 12/7/18**
6	**1.4.2.1**		**Design**	**Mon 8/24/1**	**Fri 6/22/18**
13	**1.4.2.2**		**Production**	**Mon 4/2/18**	**Fri 11/9/18**
19	**1.4.2.3**		**testing**	**Mon 11/12/**	**Fri 12/7/18**
22	**1.4.3**		**SiTracker**	**Mon 8/24/1**	**Fri 1/4/19**
23	**1.4.3.1**		**Design**	**Mon 8/24/1**	**Fri 7/22/16**
28	**1.4.3.2**		**protoype**	**Mon 8/24/1**	**Fri 6/23/17**
151	**1.4.3.3**		**production**	**Mon 12/26/**	**Fri 1/4/19**
322	**1.4.4**		**Assembly/test/integration**	**Tue 12/25/1**	**Mon 3/18/1**
323	**1.4.4.1**		**SiTracker Assembly**	**Tue 12/25/1**	**Fri 1/11/19**
329	**1.4.4.2**		**install electronics**	**Fri 1/11/19**	**Fri 2/1/19**
334	**1.4.4.3**		**Pre-Installation to IR**	**Mon 2/4/19**	**Mon 3/18/1**
339	**1.4.5**		**SiTracker electronics**	**Thu 12/1/16**	**Fri 5/17/19**
340	**1.4.5.1**		**FPHX**	**Thu 12/1/16**	**Wed 8/9/17**
348	**1.4.5.2**		**ROC prepro**	**Sat 4/1/17**	**Fri 9/15/17**
353	**1.4.5.3**		**ROC production**	**Fri 6/1/18**	**Thu 10/18/1**
358	**1.4.5.4**		**FEM**	**Sat 12/1/18**	**Fri 5/17/19**